**Summer14!IN THE UNITED STATES DISTRICT COURT**
**FOR THE EASTERN DISTRICT OF TEXAS**
**MARSHALL DIVISION**

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| OPTI, INC., | § | |
| | § | |
| *Plaintiff*, | § | |
| | § | |
| *v.* | § | CASE NO. 2:10-CV-00279-JRG |
| | § | |
| VIA TECHNOLOGIES, INC. and VIA TECHNOLOGIES, INC. (Taiwan), | § | |
| | § | |
| *Defendants*. | § | |

**MEMORANDUM OPINION AND ORDER**

Before the Court are the post-trial motions of VIA Technologies, Inc. and VIA Technologies, Inc. (Taiwan) (collectively, "VIA") (Dkt. Nos. 321, 322, 324, 325, and 326). Having considered these motions and the briefings of the parties, the Court finds that each of these motions should be **DENIED**, for the reasons set forth below.

## I. BACKGROUND AND PROCEDURAL HISTORY

Plaintiff OPTi, Inc. ("OPTi") filed this suit for patent infringement on July 30, 2010, alleging infringement of U.S. Patent Nos. 5,710,906 ("the '906 Patent") and 6,405,291 ("the '291 Patent"). Over the course of the litigation, OPTi dropped its allegations with respect to the '291 Patent. The case went to trial on the '906 Patent on May 28, 2013. Following a four-day trial, the jury returned a unanimous verdict finding that VIA directly infringed claim 26 of the '906 Patent, and that VIA indirectly infringed claim 26 of the '906 Patent by inducing infringement (Dkt. No. 274). The jury further found that claim 26 of the '906 Patent was not invalid, and found damages in the amount of $2,111,905.40. *Id.* The jury also found that OPTi had not

proven willful infringement of the '906 Patent. *Id.* At the conclusion of the jury trial, the Court held a bench trial on VIA's defenses of laches and equitable estoppel, and denied those defenses (Dkt. No. 303). The Court entered final judgment on September 9, 2013 (Dkt. No. 308).

The patent-in-suit is sometimes referred to by OPTi as a "Pre-Snoop Patent." In general, the patent relates to cache memory, which is a special, temporary memory that can be used, for example, with a central processing unit ("CPU"). Reading data from the cache is faster than reading data from main memory. The cache can thereby improve the performance of the CPU and other devices. Some devices can access main memory without passing the data through the CPU by using a feature known as Direct Memory Access ("DMA"). The terms "inquire" and "snoop" both refer to checking for consistency between data in the cache and corresponding data in main memory. If the data in the cache has been modified, then the corresponding data in the main memory should be updated before that data in main memory is accessed, for example by a DMA device. Devices communicate with each other, with memory, and with the processor over one or more buses, such as the Peripheral Component Interconnect ("PCI") bus.

The Abstract of the '906 Patent reads:

> When a PCI-bus controller receives a request from a PCI-bus master to transfer data with an address in secondary memory, the controller performs an initial inquire cycle and withholds TRDY# to the PCI-bus master until any write-back cycle completes. The controller then allows the burst access to take place between secondary memory and the PCI-bus master, and simultaneously and predictively, performs an inquire cycle of the L1 cache for the next cache line. In this manner, if the PCI burst continues past the cache line boundary, the new inquire cycle will already have taken place, or will already be in progress, thereby allowing the burst to proceed with, at most, a short delay. Predictive snoop cycles are not performed if the first transfer of a PCI-bus master access would be the last transfer before a cache line boundary is reached.

The Court has previously construed the '906 Patent, and a description from a prior case will be helpful and instructive:

> The OPTi patents relate to "core logic" chipsets, the processors that direct traffic between the central processor, memory, input/output devices, graphics cards, video cards, and various other devices that are contained within, or connected to, a computer. . . .
>
> In the earliest days of computer processing, there were no core logic chipsets. The central processor communicated directly with peripheral devices that made up the computer. As computers got more complicated, chipsets were introduced as a way of coordinating the burgeoning array of functionality and relieving central processors of that administrative burden. This freed more CPU resources for the fundamental mission of computing.
>
> Broadly speaking, a typical chipset operates as an input/output (I/O) hub for the CPU, memory, peripherals, etc. . . .
>
> The links between the various devices comprising the computer, known as interfaces, consist of conductors on which the devices transmit signals to one another, communicating address, command, and data information. The most common type of interface is known as a bus. The buses and interfaces allow the various computer devices to exchange data and to operate in coordination with one another.
>
> . . . .
>
> The Pre–Snoop patent[] addressed a[n] issue that arose with the introduction of the PCI bus and the subsequent development of the Pentium and Pentium-compatible processors. One of the advantages of the PCI was its ability to transfer data from one device to another by a particular method called "burst" transfers. The Pre–Snoop patents disclose a technique for optimizing such burst transfers with Pentium processors.
>
> Data is stored, created or used at a lot of places in a computer. Each such location is known as an address. For example, a memory storage device containing data to be read (the "target") cannot know that it is being asked to transfer data or what data to transfer unless and until the requesting device (the "master") puts an address onto the bus notifying the target that it is the object of a request and notifying the target what data is being requested. In a "burst" transfer, this information is all that the target needs to figure out which data to transfer, as the target dispatches data until the target is told to stop by the master or elects to stop the transaction itself.

A complication arises in this scenario because much of the memory can be stored in two places: main memory or cache memory. Cache memory is memory that stores copies of information expected to be used by the CPU at addresses that correspond to addresses for that information in secondary memory. This memory typically operates at particularly high speed and is typically positioned adjacent to the CPU. Access to the cache is thus generally quicker than access to the main memory. This speeds up the CPU's ability to access and process the data that it needs.

As the CPU processes data, it saves that data to the cache for continued convenient access. The problem is that the CPU may well change the data that it is processing. If that modified data is stored only in the cache, it will not be identical to the data stored on, for example, the disk drive from which it was initially read. Thus, if some other device—a CD drive, for example—accesses the main memory to read data, it may get data that is no longer current.

In Intel's X86 line of CPU's, the system solved this problem by using a "write-through" cache. Basically, as data was modified by the CPU, it was written to both the main and cache memories, thereby assuring constant "cache consistency." In the Pentium processors, the cache was a "write-back" cache. This meant that the CPU did not take the time to write every modification through to main memory. Instead, modified data was stored in the cache with a flag to indicate its modified state. Thus, to read data from memory in a Pentium system, it was necessary to adopt some mechanism to check for the presence of this flag, to assure that the data in main memory was valid, and that the cache did not contain a version of data that had been modified by the CPU.

The mechanism adopted was a "snoop." For example, a bus master seeking to initiate a transaction would first initiate an "inquire" or "snoop" cycle to the CPU to find out whether the data being sought had been stored in cache memory in a modified state and to "write back" the most current version of the data to the main memory if a modification had been made.

The PCI standard required one "line" of cache memory to be snooped at a time, and then permitted transfer of that line if the snoop showed it to be either absent from the cache or in the cache but unmodified. The PCI protocol required that a transfer stop at the end of each line transferred, snoop the next line, transfer the line just snooped, and then stop again to snoop the succeeding line. Because burst transfers could encompass any amount of data, including data stored in multiple lines of memory, this practice resulted in a non-uniform transfer in which the bus spent more time sitting idle than it did carrying data.

The sole exception to this rule was that multiple lines of memory could be read without stopping when the data to be transferred was not cacheable. In this instance, the snoop operation could be ignored because there was no risk of stale

> data being accessed. Thus, the entire burst of data could be sequentially pre-fetched and read to the master without interruption.
>
> The Pre–Snoop patent[] embod[ies] the idea that cacheable memory could be transferred nearly as rapidly as non-cacheable memory if the snoop of a line were conducted while the preceding line was transferring. In that way, as in the case of non-cacheable memory, the system would know that the line was not stale and there would be no need to stop the transfer at the end of the first line to snoop the second line because that snoop would already be completed. The "snoop ahead" process could be repeated as long as the burst transfer was underway so that all of the data comprising the burst could be sent without interruption and at a constant rate.

*OPTi Inc. v. nVidia Corp.*, Case No..2:04-CV-377-TJW, 2006 WL 1133331, at *3-6 (E.D. Tex. Apr. 24, 2006).

Claim 26 of the '906 Patent claims:

> Apparatus for transferring data between a bus master and a plurality of memory locations at respective addresses in an address space of a secondary memory, for use with a host processing unit and a first cache memory which caches memory locations of said secondary memory for said host processing unit, said first cache memory having a line size of 1 bytes, comprising:
>
> means for sequentially transferring at least three data units between said bus master and said secondary memory beginning at a first starting memory location address in said secondary memory address space and continuing sequentially beyond a 1-bye boundary of aid secondary memory address space; and
>
> means for, prior to completion of the transfer of the first data unit beyond said 1-byte boundary, determining whether an N+1'th 1-byte line of said secondary memory is cached in a modified state in said first cache memory, said N+1'th 1-byte line being the line of said secondary memory which includes said first data unit beyond said 1-byte boundary,
>
> said means for sequentially transferring, transferring all of said data units at a constant rate.

('906 Patent 34:63-35:16). The accused products are VIA chipsets that the jury found infringed the '906 Patent.

In its post-trial motions, VIA petitions the Court for judgment as a matter of law (JMOL) or, in the alternative, for a new trial, on the grounds that (1) The '906 Patent is invalid (Dkt. No. 322); (2) VIA did not literally infringe the '906 Patent (Dkt. No. 321); (3) VIA did not infringe the '906 Patent under the doctrine of equivalents, or indirectly (Dkt. No. 324); (4) the Court erred in its construction of the term "constant rate" in the '906 Patent (Dkt. No. 325); and (5) the Court erred in instructing the jury regarding "equivalents" under 35 U.S.C. §112(6).

## II. GENERAL LEGAL STANDARDS

Judgment as a matter of law is only appropriate when "a reasonable jury would not have a legally sufficient evidentiary basis to find for the party on that issue." Fed. R. Civ. P. 50(a). Procedural standards for JMOL flow from the law of the regional circuit. *Finisar Corp. v. DirectTV Group, Inc.*, 523 F.3d 1323, 1332 (Fed. Cir. 2008). The Fifth Circuit "uses the same standard to review the verdict that the district court used in first passing on the motion." *Hiltgen v. Sumrall*, 47 F.3d 695, 699 (5th Cir. 1995). Thus, a jury verdict must be upheld, and judgment as a matter of law may not be granted, unless "the facts and inferences point so strongly and overwhelmingly in favor of one party that the court concludes that reasonable jurors could not arrive at a contrary verdict." *Bellows v. Amoco Oil Co.*, 118 F.3d 268, 273 (5th Cir. 1997). The jury's verdict must be supported by "substantial evidence" in support of each element of the claims. *Am. Home Assurance Co. v. United Space Alliance*, 378 F.3d 482, 487 (5th Cir. 2004).

In considering whether JMOL is appropriate, a court reviews all evidence in the record and must draw all reasonable inferences in favor of the nonmoving party; however, a court may not make credibility determinations or weigh the evidence, as those are solely functions of the jury. *See Reeves v. Sanderson Plumbing Prods., Inc.*, 530 U.S. 133, 150-51 (2000); *Med. Care Am., Inc. v. Nat'l Union Fire Ins. Co.*, 341 F.3d 415, 420 (5th Cir. 2003).

Under Rule 59(a) of the Federal Rules of Civil Procedure, a new trial can be granted to any party to a jury trial on any or all issues "for any reason for which a new trial has heretofore been granted in an action at law in federal court." Fed. R. Civ. P. 59(a). "A new trial may be granted, for example, if the district court finds the verdict is against the weight of the evidence, the damages awarded are excessive, the trial was unfair, or prejudicial error was committed in its course." *Smith v. Transworld Drilling Co.*, 773 F.2d 610, 612-13 (5th Cir. 1985). The Court must view the evidence "in a light most favorable to the jury's verdict, and . . . the verdict must be affirmed unless the evidence points so strongly and overwhelmingly in favor of one party that the court believes that reasonable persons could not arrive at a contrary conclusion." *Dawson v. Wal-Mart Stores, Inc.*, 978 F.2d 205, 208 (5th Cir. 1992).

## III. VALIDITY OF THE '906 PATENT (Dkt. No 322)

If the '906 Patent is invalid, the Court need not reach the remaining issues of infringement. Accordingly, the Court will address this issue first. VIA argues that claim 26 of the '906 Patent is invalid because (1) it was anticipated by VIA's VT82C505 Chip ("the 505 chip"); (2) the claim is indefinite under 35 U.S.C. § 112; and (3) the patent fails to meet the enablement and written description requirements of 35 U.S.C. § 112.

### A. Legal Standards

A patent is "presumed to be valid and invalidity must be proven by clear and convincing evidence." *OSRAM Sylvania, Inc. v. Am. Induction Techs., Inc.*, 701 F.3d 698, 704 (Fed. Cir. 2012). "A patent claim is anticipated if each and every limitation is found in a single prior art reference." *Id.* (citing 35 U.S.C. § 102). It is "axiomatic" that a device "which would literally infringe if later anticipates if earlier." *Bristol-Meyers Squibb Co. v. Ben Venue Labs., Inc.*, 246 F.3d 1368, 1378 (Fed. Cir. 2001). With a claim element expressed as a means plus function,

"absent structure in a prior art reference which is capable of performing the functional limitation of the means, the prior art reference does not meet the claim." *RCA Corp. v. Applied Digital Data Systems, Inc.*, 730 F.2d 144, 1444 (Fed. Cir. 1984). An accused device may infringe if it is "reasonably capable of satisfying the claim limitations," but does not infringe if "it does not infringe in its normal configuration, even if it may be altered into an infringing configuration under unusual circumstances." *Hilgraeve Corp. v. Symantec Corp.*, 265 F.3d 1336, 1343 (Fed. Cir. 2001) (summarizing *High Tech Med. Instrumentation, Inc. v. New Image Indus., Inc.*, 49 F.3d 1551, 1556 (Fed. Cir. 1995)). By analogy, then, in order to anticipate a patent claim, prior art must be "reasonably capable" of meeting each and every claim limitation "in its normal configuration"—absent "unusual circumstances."

35 U.S.C. § 112 requires that a patent's specification "conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the inventor or a joint inventor regards as the invention." Indefiniteness is "a legal conclusion that is drawn from the court's performance of its duty as the construer of patent claims . . . . a court may consider or reject certain extrinsic evidence in resolving" indefiniteness disputes, but "the court is looking to the extrinsic evidence to assist in its construction of the written document." *Exxon Research and Eng'g Co. v. U.S.*, 265 F.3d 1371, 1376 (Fed. Cir. 2001) (abrogated on other grounds by *Nautilus*, 134 S. Ct. 2120, 2124 (2014)). A patent is invalid for indefiniteness "if its claims, read in light of the specification delineating the patent, and the prosecution history, fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention." *Nautilus*, 134 S. Ct. at 2124.

35 U.S.C. § 112 also requires that "the specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise,

and exact terms as to enable any person skilled in the art to which it pertains . . . to make and use the same." The enablement requirement "is satisfied when one skilled in the art, after reading the specification, could practice the claimed invention without undue experimentation." *AK Steel Corp. v. Sollac & Ugine*, 344 F.3d 1234, 1244 (Fed. Cir. 2003).

Apart from the enablement requirement, the Federal Circuit has also identified a separate written description requirement in § 112—the specification must contain "a written description of the invention" in addition to the enablement description of "the manner and process of making and using" the invention. *Ariad Pharms., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336 (Fed. Cir. 2010). This description must not merely define the outer boundaries of the claim, but must "reasonably convey[] to those skilled in the art that the inventor had possession of the claimed subject matter as of the filing date. *Id.* at 1351.

B. Anticipation

VIA first argues that the evidence at trial unambiguously establishes that its 505 Chip, which predated the application date of the '906 Patent, *could* be configured in a manner that would meet all the elements of claim 26 of the '906 Patent. VIA assumes that, if these facts are uncontested, then it prevails as a matter of law. VIA has misapplied the legal standard for anticipation, however: in order to invalidate the patent-in-suit, the 505 chip must have been *reasonably capable* of operating in such a way as to meet each limitation of the '906 Patent. *Hilgraeve*, 265 F.3d at 1343. If the 505 chip could only be cajoled into meeting the limitations of the patent-in-suit under "unusual circumstances"—such as a directed, post-hoc attempt to replicate certain conditions in order to avoid liability for patent infringement—then it does not anticipate the '906 patent. *See id.*

A reasonable jury could easily have found that VIA's evidence failed to establish by clear and convincing evidence that the 505 chip was reasonably capable or practicing each limitation of the '906 Patent. In particular, there is no evidence that normal operation of the 505 chip provided for "transferring all of said data units at a constant rate" ('906 Patent 35:15-16). Rather, VIA demonstrated only that the 505 chip *could*, with considerable experimentation, be configured in a manner that met each of the claim limitations (Dkt. No. 322, at 9-12). This configuration was only *demonstrated* in 2001, when OPTi was in negotiations with VIA as to licensing of its pre-snoop patents (Dkt. No. 322-5).

The jury heard evidence that the 505 chip, as configured "out of the box," did not satisfy the constant rate transfer limitation of the '906 Patent (Dkt. No. 342-1, at 117-18). OPTi presented evidence that reproducing the constant rate limitation required choosing one of more than a trillion different possible combinations of configuration settings. *Id.* at 115. Dr. Alan J. Smith, one of OPTi's expert witnesses testified that it would be "essentially impossible" that anyone *actually* configured the 505 chip to meet the limitations of the '906 Patent prior to the patent's application date. More importantly, Dr. Smith testified that "there's no indication that anyone knew the proper register settings to obtain this behavior nor that they would be motivated to find them . . . ." (Dkt. No. 342-2, at 124-25). In order to anticipate the '906 Patent's limitations, then, a person of ordinary skill in the art would have had to select the correct settings from over a trillion possible combinations—without the disclosure provided by the patent itself.

OPTi likens VIA's argument to an argument that "a specialized computer chip is anticipated by a general purpose computer because the general purpose computer could have been programmed to behave like the specialized one" (Dkt. No. 342, at 6). This Court agrees. Without the disclosure provided by the '906 Patent, the 505 chip was not *reasonably capable* of

meeting the limitations set out in the '906 Patent. Ample evidence was presented in trial to this effect, and the Court has no basis on which to overturn the jury's verdict of no invalidity on this ground.

C. Indefiniteness

VIA next argues that the Court should grant judgment as a matter of law that the '906 Patent is invalid because it is indefinite. Specifically, VIA argues that the means plus function terms of claim 26 of the '906 Patent fail to identify a corresponding structure that would render the term sufficiently definite under *Biomedino, LLC v. Waters Techs.*, 490 F.3d 946, 948 (Fed. Cir. 2007).

The Court notes, as a preliminary matter, that this is not a motion for JMOL under rule 50(a), which requires that "a party has been fully heard on an issue during a jury trial." Indefiniteness is a matter of law, to be decided by the Court. *Exxon*, 265 F.3d at 1376. No question of indefiniteness was presented to the jury, and the jury was not instructed on indefiniteness. *See* Dkt. No. 295, at 18-56. The parties have already had an opportunity to present arguments and evidence concerning indefiniteness at the Court's *Markman* hearing, and the Court has construed the disputed claims to be not indefinite (Dkt. No. 150, at 32, 39).

This portion of VIA's motion must be treated, and charitably so, as a motion to reconsider the Court's *Markman* Order in light of evidence presented at trial. To prevail on a motion for reconsideration, a party must "clearly establish either a manifest error of law or fact or must present newly discovered evidence." *Ross v. Marshall*, 426 F.3d 745 (5th Cir. 2005). Such motions "cannot be used to raise arguments which could, and should, have been made before the judgment issues." *Id.* VIA has failed to demonstrate why the evidence it presented at trial could not have been presented to the Court before or as a part of claim construction.

Moreover, by presenting its evidence at trial, rather than at the appointed time, VIA effectively ambushes OPTi by using trial evidence—directed at issues presented to the jury—in support of its already-resolved, purely legal arguments. OPTi cannot be expected to anticipate this line of argument and rebut it at trial.[1]

The Court thus finds that reconsideration of its decision is inappropriate here. VIA has offered no new evidence that could not have been presented before the Court ruled on the issue of indefiniteness. Even so, out of an abundance of caution the Court will note that it has read and considered VIA's arguments and finds them unconvincing on the merits.

VIA also advances a new argument, not presented during claim construction, that the term "constant rate" is indefinite in light of *Nautilus*, 134 S. Ct. at 2124. Though that term may be "amenable to construction" and not "insolubly ambiguous," VIA argues, it does not inform a person of ordinary skill in the art "with reasonable certainty" what is claimed (Dkt. No. 366, at 3). This argument is unavailing. Though the Court rejected both parties' proposed constructions for the term "constant rate," it nonetheless had no trouble construing the term with specificity (Dkt. No. 150, at 25).

VIA's arguments regarding indefiniteness must therefore be rejected.

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[1] VIA cites the concurring opinion of Judge Dyk in *Oakley, Inc. v. Sunglass Hut International*, 316 F.3d 1331, 1347 (Fed. Cir. 2003), in support of the proposition that the Court should reopen questions of claim construction in light of testimony offered at trial. That case, however, did not squarely address the question here: *Oakley* examined the propriety of a grant of preliminary injunction, and found that the Defendant had not proven at that stage of the proceedings that the patent-in-suit was invalid. There is no indication in *Oakley* that, had the district court in that case held a full *Markman* hearing and construed the patent-in-suit, the district court would be required to revisit that ruling post-trial. The whole point of a *Markman* hearing is to "determine the meaning of claim terms" for the duration of the district court's case. Defendant's objections to the Court's claim construction order are best taken up on appeal, rather than in post-trial motions.

D. Written Description and Enablement

Finally, VIA argues that the '906 Patent fails to meet the Patent Act's enablement and written description requirements. First, VIA argues that the testimony of VIA's expert, Mr. Joe McAlexander, conclusively established that a person of ordinary skill in the art would not have been able to implement the claimed invention because of a lack of description of certain signals in the patent's Figure 8, and because the "data path" limitation would require undue experimentation (Dkt. No. 322, at 20-24). This testimony, however, was directly contradicted by OPTi's expert, Dr. Smith (Dkt. No. 322-18, at 130-132). The jury had ample evidence supporting its reasonable conclusion that VIA did not prove by clear and convincing evidence that the '906 Patent was invalid for failure meet the written description and enablement requirements. The jury clearly had evidence of opposing natures and obviously weighed the evidence such that it accepted OPTi's position and rejected VIA's. This is the essence of the jury's function.

Having concluded that each of VIA's arguments regarding the validity of the '906 Patent are unavailing, the Court finds ample evidence in the record supporting the jury's finding that the '906 Patent is not invalid, and that finding must stand.

## IV. LITERAL INFRINGEMENT OF THE '906 PATENT (Dkt. No. 321)

VIA argues that the jury's verdict of direct infringement is not supported by the evidence at trial. First, it asks the Court to grant JMOL or declare a new trial on the basis that VIA did not *literally* infringe the '906 Patent (Dkt. No. 321); VIA's arguments on infringement under the doctrine of equivalents and indirect infringement are filed in a separate motion (Dkt. No. 324). The Court notes, as a preliminary matter, that a new trial or a JMOL of no *direct* infringement is *only* required if VIA demonstrates that the evidence supports *neither* literal direct infringement *nor* infringement under the doctrine of equivalents, since the Court must uphold the jury's

verdict if it has any reasonable basis to do so from the evidence. *See* Section II, *supra*. The Court will address VIA's literal infringement arguments first.

A. First Cache Memory

VIA first argues that the evidence establishes that the accused products do not meet the limitation of "determining whether an N+1'th 1-byte line of said secondary memory is cached in a modified state in said first cache memory" ('906 Patent 35:10-13) The Court construed the term "first cache memory" to mean "the first level of cache memory, commonly referred to as L1 cache memory" (Dkt. No. 150, at 20). VIA argues that the representative processing units have both an L1 and an L2 cache, and that the evidence shows that the accused chip products cannot distinguish between modified states cached in the L1 cache and modified states in the L2 cache. Presented with a "hit modified condition," then, as the result of a snoop, the accused products cannot determine whether the modified data is in the L1 or the L2 cache of the processor. Accordingly, VIA argues, the accused products cannot "determin[e] whether" a line of memory is "cached in a modified state in said *first* cache memory" (i.e., the L1 cache), as opposed to the L2 cache.

VIA's argument misreads the "determining whether" limitation of the patent. The point of the "determining whether" limitation is that the accused chip product must perform a snoop that warns the chip if there exists change in the sought data that is cached in the L1 cache. In other words, the limitation is satisfied if the following condition holds true for the accused product:

> If there an N+1'th 1-byte line of said secondary memory is cached in a modified state in said first cache memory, then the accused product is alerted.

VIA reverses the direction of this conditionality, arguing that the "determining whether" limitation must distinguish between changes cached in the L1 cache and changes cached in the L2 cache. Under VIA's hypothetical reading, the limitation sets forth a different conditional:

> If the accused product is alerted, then the N+1'th 1-byte line of said secondary memory is cached in a modified state in said first cached memory.

This reading subverts the most reasonable reading of the patent, which involved snooping the cache for changed data prior to the completion of the previous line of data transfer. The snoop's function is to determine whether modified data exists in the cache; the process of resolving changes, in which the location of modified data becomes important, is outside the scope of claim 26.[2]

OPTi presented ample evidence at trial that the accused products snoop ahead to determine whether the L1 cache contains a modified version of sought data, and that, if a modification exists, a "hit end pound signal will signal that," and that the L1 cache of the representative products was snooped "to determine if it contains a version of a line of data that is different from the version in secondary memory" (Dkt. Nos. 341-3, at 14; 341-2, at 90). The evidence thus supports a finding by the jury that the accused products meet the "first cache memory" limitation of claim 26.

[2] The Court also notes that VIA had ample opportunity to advocate for a specific construction of this claim element at its *Markman* hearing, and did not suggest a particular construction. VIA's newly-raised claim construction dispute thus comes without warning to OPTi, who reasonably adopted the Court's interpretation at trial and tailored its presentation of the evidence to that interpretation.

B. "Host Processing Unit" and Similar Limitations

VIA next argues that the accused chip products themselves lack a "host processing unit," a "first cache memory," and "secondary memory," and thus do not meet the limitations of claim 26 of the '906 Patent. The relevant claim language claims an

> [a]pparatus *for* transferring data between a bus master and a plurality of memory locations at respective addresses in an address space of a secondary memory, *for use with* a host processing unit and a first cache memory which caches memory locations of said secondary memory for said host processing unit, said first cache memory having a line size of 1 bytes, *comprising* . . . .

('906 Patent 34:63-35:2).

Obviously, by its terms the claimed apparatus need not itself contain a host processing unit, a first cache memory, or a secondary memory. It need merely be designed for use with those components, and meet the means plus function limitations that follow the "comprising" term. *Cf. STX, LLC v. Brine, Inc.*, 211 F.3d 588, 591 (Fed. Cir. 2000) (quoting *Rowe v. Dror*, 112 F.3d 473, 478 (Fed. Cir. 1997) ("'[W]here a patentee defines a structurally complete invention in the claim body and uses the preamble only to state a purpose or intended use for the invention, the preamble is not a claim limitation.'")). In this case, obviously, the components listed in the preamble are limiting, inasmuch as the *structures* claimed must be designed for systems comprising a host processing unit, a first cache memory, and a secondary memory in order for the claim terms to make sense. It should be clear, however, that the claimed apparatus itself need only communicate with these structures, rather than incorporate them into the body of the apparatus. VIA's argument thus stands on a misreading of the claims of the '906 Patent and is not a proper ground for JMOL or new trial.

C. Equivalent Structure Analysis Under 35 U.S.C. § 112(6)

VIA next argues that JMOL or new trial is required because OPTi failed to present sufficient evidence that the accused products contain structures that are "equivalent" under 35 U.S.C. § 112(6) to the corresponding structures identified by the Court for each of claim 26's means plus function terms. VIA argues that equivalence for the purpose of § 112(6) may only be demonstrated by "side-by-side comparison of the corresponding structures and the structures of [a]ccused [d]evices" (Dkt. No. 321, at 7).

The crux of the motion is the Federal Circuit's "function-way-result" test, which the Court set before the jury as one measure of the statutory equivalence required for a finding of infringement. A structure in an accused product identified for purposes of a means plus function term is equivalent if it performs a function that is identical to the function claimed, and it performs that function in substantially the same way as the specified structure, with substantially similar results. *See Odetics, Inc. v. Storage Technology Corp.*, 185 F.3d 1259, 1267 (Fed. Cir. 1999).

The record is replete with evidence that structures in the accused products perform functions identical to those specified in the two means plus function limitations of claim 26, and that these structures perform the claimed functions in substantially the same way as the specified structures, with substantially the same results. *See* Dkt. No. 341-2, at 157-62 & 173-82 ("means for sequentially transferring . . ." limitation); *id.* at 162-67 & 182-89 ("means for . . . determining . . ." limitation). OPTi's expert witness dutifully identified the function, way, and result for each of the means plus function limitations, and compared them to the accused products.

VIA argues that OPTi's expert's "way" analysis was insufficient to support a finding of equivalence. Its argument is rooted in the assertion that proving equivalence under 35 U.S.C. §

112 requires a "way" analysis that entails "a detailed structural comparison of how the corresponding and accused structures each operate to exactly perform the claimed function" (Dkt. No. 321, at 10). VIA accuses OPTi of glossing over the "way" analysis with a "black box" that obscures substantial differences between the specified structures and those used by the accused products. *Id.*

VIA demands a level of specificity in OPTi's "way" analysis that is unsupported by the law. In *Odetics*, the Federal Circuit explicitly held that "a component-by-component analysis of structural equivalence" is not required. 185 F.3d at 1268. Presented with clearly sufficient expert testimony of equivalence, VIA cannot obtain JMOL simply by demanding another and further level of specificity, much like a young child repeatedly asking a parent "but why" after each successive explanation. VIA was free to and did cross-examine the testimony of OPTi's expert to expose flaws in his analysis, and to put on the testimony of its own witnesses. The jury, in its turn, was free to credit each side's testimony or not, and the Court finds no cause here to second guess the jury's findings or how they weighed this particular evidence. As stated above, weighing competing evidence and selecting which they find most credible is the essence of the jury's function within our legal system. This Court will not infringe upon that function.

D. Internal PCI Bus

Finally, VIA argues that OPTi's expert's testimony failed to demonstrate that the accused products transferred data over an internal PCI bus. On this point, VIA merely pits the testimony of its own expert against the testimony of OPTi's expert (Dkt. No. 321, at 27-28). The gist of this argument seems to be that VIA's expert's testimony is derived from personal knowledge of the accused products, and is thus more reliable than the testimony of OPTi's expert, which draws conclusions from documentary evidence. *See* Dkt. No. 341-2, at 190-200. All that need be said

about this argument is that the jury could reasonably have credited the testimony of OPTi's expert over the testimony of VIA's expert. VIA's argument must therefore be rejected.

## V. INFRINGEMENT UNDER THE DOCTRINE OF EQUIVALENTS (Dkt. No. 324)[3]

Having determined that the jury's verdict finding direct infringement could stand on a finding of literal infringement, and that neither JMOL of no infringement nor a new trial is required on this basis, it is not strictly necessary for the Court to address VIA's petition for JMOL of no infringement under the doctrine of equivalents (Dkt. No. 324). Out of an abundance of caution, however, the Court will briefly address this issue.

VIA raises two arguments unique to the doctrine of equivalents. First, it alleges that, because "snoops," "pre-snoops," and PCI bursts were known at the time of the invention, the accused products (which use snoops, pre-snoops, and PCI bursts) are not "after-arising technology," and thus cannot infringe under the doctrine of equivalents. Here, VIA simply misstates Federal Circuit law.

"Although an equivalence analysis under § 112[6] and the doctrine of equivalents are not coextensive . . . and have different origins and purposes, their tests for equivalence are closely related." *Chiuminatta Concrete Concepts, Inc. v. Cardinal Industries, Inc.*, 145 F.3d 1303, 1310 (Fed. Cir. 1998). "Both § 112[6] and the doctrine of equivalents protect the substance of a patentee's right to exclude by preventing mere colorable differences or slight improvements from

[3] Though VIA presented its doctrine of equivalents arguments in the same motion as its arguments regarding induced infringement, the two issues are logically distinct and the Court will address VIA's inducement arguments in the next section.

escaping infringement . . . ." *Id.* The doctrine of equivalents, however, differs somewhat from equivalence analysis under § 112(6). The doctrine protects patent holders in the event that

> a variant of an invention may be developed after the patent is granted, and that variant may constitute so insubstantial a change from what is claimed in the patent that it should be held to be an infringement. Such a variant, based on after-developed technology, could not have been disclosed in the patent.

*Id.* Technology that predates the invention thus does *not* infringe under the doctrine of equivalents, *if it is also substantially different under 35 U.S.C. § 112(6). Id.* at 1311. That is to say, an accused product may infringe under the doctrine of equivalents without infringing under s 112(6), if and only if the "substantial difference" that takes the accused product out of §112(6) liability stems from a new variant of the technology that, in light of the development of the technology post-patent, is not substantial. It does not follow, however, that "[w]here . . . the accused structures are not 'after arising technology,' the doctrine of equivalents is not available (Dkt. No. 324, at 1). An accused product that *does* use an equivalent structure under § 112(6) may obviously *also* infringe under the doctrine of equivalents.

The Court has already determined that the jury could have found that the accused products contain structures equivalent to those claimed under § 112(6). This conclusion nullifies VIA's argument about after-arising technology, since the rule of *Chiuminatta* depends on the assumption that there is no equivalence under § 112(6). This portion of VIA's argument must thus be rejected.

In addition to its arguments concerning after-arising technology, VIA raises several arguments going to the sufficiency of OPTi's evidence regarding the doctrine of equivalents. These arguments rehash the arguments discussed above regarding OPTi's §112(6) analysis. The

Court relies on its discussion above to demonstrate the sufficiency of OPTi's function-way-result evidence.

VIA's arguments regarding the doctrine of equivalents must thus be rejected.

## VI. INDUCED INFRINGEMENT (Dkt. No. 324)

Next, VIA argues that OPTi failed to produce sufficient evidence of specific intent to support the jury's finding of induced infringement (Dkt. No. 324). Its argument on this point can be reduced to an assertion that the evidence demonstrates unequivocally VIA's good-faith belief that the '906 Patent was invalid. At trial, OPTi presented substantial evidence indicating that the accused products infringe "out of the box" using their default settings; that VIA advertised the infringing features of its products to customers; and that VIA's customers use the accused products to infringe (Dkt. No. 339-2, at 200-203). It is undisputed that VIA knew of the '906 Patent during the relevant infringement period and engaged in licensing negotiations. The jury heard extensive evidence regarding these negotiations, VIA's defense of invalidity, and the reasonableness of that defense (*e.g.*, Dkt. No. 292, at 69-125; Dkt. No. 294, 105-35). The jury was instructed to consider whether VIA had a good-faith belief in the invalidity of the '906 Patent during its deliberations, as bearing on OPTi's induced infringement claim. Evidently, the jury nonetheless concluded that VIA was liable for induced infringement. The Court sees no reason, given the evidence, to question the jury's factual findings, and VIA's arguments on induced infringement requesting JMOL or a new trial must be denied.

## VII. CLAIM CONSTRUCTION

Next, VIA argues that the Court erred in its construction of the term "constant rate," and that a new trial should be granted on this basis. For the reasons outlined in the Court's claim construction Order, the Court rejects VIA's proposed construction of that term and reaffirms its

prior construction (Dkt. No. 150, at 25). Accordingly, the Court finds that its instructions to the jury regarding construction of the term "constant rate" were correct, and VIA's motion should be denied.

## VIII. EQUIVALENTS INSTRUCTION

Finally, VIA argues that the Court presented the jury with a faulty instruction on equivalence under 35 U.S.C. § 112(6). The Court instructed the jury that

> [a] structure may be found to be equivalent to one of the corresponding structures I have defined as being described in the ‘’906 Patent if at the time the ‘906 Patent issued a person having ordinary skill in the field of technology of the ‘906 Patent either would have considered the differences between the corresponding structures to be insubstantial or would have found the structures performed the function in substantially the same way to accomplish substantially the same result.

(326-1, at 30-31). VIA takes issue with the use of "or" in this instruction, arguing that the Court should have instructed the jury that the exclusive test for equivalence is insubstantial difference, and that the function-way-result test is merely "a tool" for determining whether the insubstantial differences test is met (Dkt. No. 326, at 2).

A motion for new trial on the basis of an erroneous instruction should be granted if the charge creates "substantial and ineradicable doubt whether the jury has been properly guided in its deliberations." *Z4 Techs., Inc. v. Microsoft Corp.*, 507 F.3d 1340, 1353 (Fed. Cir. 2007) (citing *Hartsell v. Doctor Pepper Bottling Co.*, 207 F.3d 269, 272 (5th Cir. 2000)).

In *Odetics, Inc. v. Storage Technology Corp.*, the Federal Circuit made clear that the function-way-result test (or, in the § 112(6) context, the "way-result test," since the function must be identical)) is merely a gloss on the "insubstantial differences" test. 185 F.3d 1259, 1267 (Fed. Cir. 1999). There the Federal Circuit held that "[s]tructural equivalence under § 112[6] is met only if the differences are insubstantial . . . that is, if the assertedly equivalent structure

performs the claimed function in substantially the same way to achieve substantially the same result." *Id.*

The Court finds that its instruction is consistent with the law, and that its use of "or" does not create substantial doubt about whether the jury was properly guided in its deliberations. The "way-result test" is a gloss on the "insubstantial differences" test and was fairly presented to the jury as such. VIA's motion should be denied.

## IX. CONCLUSION

For the reasons set forth above:

1. VIA's Renewed Motion for JMOL of No Literal Infringement (Dkt. No. 321) is **DENIED**;
2. VIA's Renewed Motion for JMOL of Invalidity (Dkt. No. 322) is **DENIED**;
3. VIA's Renewed Motion for JMOL of No Infringement Under the Doctrine of Equivalents (Dkt. No. 324) is **DENIED**;
4. VIA's Motion for New Trial Based on Erroneous Claim Construction (Dkt. No. 325) is **DENIED**; and
5. VIA's Motion for New Trial Based on Erroneous Statutory Equivalents Instruction (Dkt. No. 326) is **DENIED**.

**So ORDERED and SIGNED this 29th day of August, 2014.**

RODNEY GILSTRAP
UNITED STATES DISTRICT JUDGE